WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device comprising:

providing a semiconductor substrate having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired;

introducing a halogen-containing impurities into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region; and

performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness at said first region and said second oxide layer thickness at said second region.

2. The method of claim 1 further comprising the steps of:

forming a first memory gate electrode on said second oxide layer thickness, said second oxide layer thickness formed on said semiconductor substrate in a memory region.

3. The method of claim 2 wherein said halogen-containing impurities introducing step comprises the step of:

masking said dielectric layer to expose said first region; and

wherein said halogen-containing impurities are introduced through said dielectric layer to said first region.

4. The method of claim 3 wherein said halogen-containing impurities introducing step comprises an ion implantation.

5. The method of claim 1 wherein said halogen-containing impurities introducing step comprises the step of introducing halogen-containing impurities into said first region and wherein said second region has substantially no halogen concentration therein.

6. The method of claim 1 wherein said halogen-containing impurities introducing step comprises the steps of introducing halogen-containing impurities into said first region at a first concentration and introducing halogen-containing impurities

into said second region at a second concentration, said first concentration greater than said second concentration.

7. The method of claim 5 wherein said halogen-containing impurities introducing step comprises an ion implantation.

8. The method of claim 1 wherein said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

9. The method of claim 1 wherein said semiconductor substrate also includes a third region where a third oxide layer thickness is desired, and wherein said halogen-containing impurities introducing step also introduces halogen-containing impurities such that a different halogen concentration is formed in said third region than in said first region or in said second region.

10. The method of claim 1 wherein said semiconductor device comprises a flash EEPROM semiconductor device.

11. The method of claim 2 wherein said first memory gate electrode comprises a floating gate electrode.

12. The method of claim 11 wherein said first memory gate electrode is part of a stack gate cell.

13. The method of claim 11 wherein said first memory gate electrode is part of a split gate cell.

14. The method of claim 2 wherein said first memory gate electrode comprises a control gate electrode.

15. The method of claim 14 wherein said first memory gate electrode is part of a stack gate cell.

16. The method of claim 14 wherein said first memory gate electrode is part of a split gate cell.

17. The method of claim 1 wherein said second oxide layer thickness is sufficiently thin to provide high driving capability for said semiconductor device comprising a flash EEPROM semiconductor device, and said first oxide layer thickness is sufficiently thick to provide high voltage reliability of said flash EEPROM semiconductor device when said flash EEPROM semiconductor device operates at a supply voltage of about ± 12 V or higher.

18. A semiconductor device fabricated according to the method of claim 1.

19. A semiconductor device fabricated according to the method of claim 10.

20. A method of forming a semiconductor integrated circuit, said method comprising steps of:

providing a semiconductor substrate, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device;

forming a gate dielectric layer comprising an oxide overlying said semiconductor substrate including said first region and said second region;

selectively implanting halogen-containing impurities into said second region; and

simultaneously forming a first thickness of dielectric material overlying said first region and forming a second thickness of dielectric material overlying said second region;

wherein said first thickness is sufficiently thin to provide high driving capability for said MOS transistor, and said second thickness is sufficiently thick to provide high voltage reliability of said high voltage device.

21. The method of claim 20 wherein said step of selectively implanting halogen-containing impurities into said first region also includes selectively implanting halogen-containing impurities into said second region such that said first region has a greater halogen concentration than said second region.

22. The method of claim 20 wherein said halogen containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities.

23 The method of claim 20 further comprising forming a third thickness of dielectric material overlying a third region, said third region being spatially apart from said first region and said second region.

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